INFORMATION DISCLOSURE CITATION

PTO-1449

Customer Number	Attorney's Dkt No.	Application No.
45114	H1494	10/674,520
	Applicant(s) Haihong Wang et al.	
	Filing Date October 1, 2003	Group 2811

U.S. PATENT DOCUMENTS

Examiner's Initials	Patent No.	Date	Name	Class	Subclass	Filing Date
	4,399,605	08-23-83	Dash et al.	29	571	02-26-82
	4,319,395	03-16-82	Lund et al.	29	571	06-28-79

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Patent No.	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered
Andrew Nguyen	10/28/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

INFORMATION DISCLOSURE CITATION PTO-1449	Customer Number 26615	ATTORNEY'S DKT NO. H1494	APPLICATION NO. Unassigned
		APPLICANT(S) Haihong Wang et al.	
		FILING DATE October 1, 2003	GROUP Unassigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AH	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
AH	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 2001 IEEE, IEDM, pages 421-424.
AH	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
AH	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
AH	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
AH	Co-pending U.S. Patent Application Serial No. 10/614,001, filed July 8, 2003, entitled: "Selective Silicidation of Gates in Semiconductor Devices to Achieve Multiple Threshold Voltages"; Shibly S. Ahmed et al.; 20 page specification, 8 sheets of drawings.

EXAMINER	DATE CONSIDERED
Andy Huynh	10/28/04

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		APPLICANT(S) Haihong WANG et al.	
		FILING DATE October 1, 2003	GROUP 2811

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
AH	6,391,750 B1	05/21/2002	Chen et al.	438	583	
	6,589,836 B1	07/08/2003	Wang et al.	438	231	
	US 2004/0038464 A1	02/26/2004	Fried et al.	438	151	
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	6,657,259 B2	12/02/2003	Fried et al.	257	350	
	US 2001/0045589 A1	11/29/2001	Takeda et al.	257	297	
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AH	US 2004/0048424 A1	03/11/2004	Wu et al.	438	154	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AH	Copy of co-pending U.S. Patent Application No. 10/857,931; by Haihong Wang et al.; filed June 2, 2004; 21 page specification; 20 sheets of drawings.

EXAMINER	DATE CONSIDERED
Andy Huynh	10/28/04

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